IN THE CLAIMS:

1. (Currently Amended) An integrated tuner comprising:

a step Automatic Gain Control (AGC) amplifier ~~(1)~~;

~~and~~ means ~~(7-11)~~ for adjusting the step AGC amplifier ~~(1)~~ only during a vertical synchronization interval.

2. (Currently Amended) ~~An integrated tuner as claimed in claim 1~~ An integrated tuner comprising: a step Automatic Gain Control (AGC) amplifier: and means for adjusting the step AGC amplifier (1) only during a vertical synchronization interval, wherein the adjusting means ~~(7-11)~~ comprise: a clock generator ~~(7)~~ for generating clock pulses; an up/down counter ~~(11)~~ for generating control signals to adjust the step AGC amplifier ~~(1)~~; means ~~(8)~~ for passing said clock pulses to said up/down counter ~~(11)~~ only during said vertical synchronization interval.

3. (Currently Amended) An integrated tuner as claimed in claim 2, wherein the adjusting means ~~(7-11)~~ further comprise: a level detector ~~(9, C1)~~ coupled to an output of the step AGC amplifier~~(1)~~; and a dual comparator ~~(10)~~ coupled to an output of said level detector to provide up/down control signals to said up/down counter ~~(11)~~ in dependence on an output signal of said level detector ~~(9, C1)~~.

4. (Currently Amended) An integrated tuner as claimed in claim 3, wherein the level detector ~~(9, C1)~~ continuously measures a total power of all signals in all channels applied to the step AGC amplifier ~~(1)~~.

5. (Currently Amended) A receiver comprising: an integrated tuner as claimed in claim 1; and an IF demodulation circuit(~~5,6~~) for providing a vertical sync signal to the integrated tuner.

6. (New) An integrated tuner comprising:

a step Automatic Gain Control (AGC) amplifier;

a synchronization slicer for separating a vertical synchronization signal from a Composite Video Broadcast Signal (CVBS) signal;

means for adjusting the step AGC amplifier only during a vertical synchronization interval output pulse period of the synchronization slicer;

wherein a width of the vertical synchronization signal output from the synchronization slicer is adjusted to control a number of pulses output to the means for adjusting the AGC amplifier.

7. (New) An integrated tuner as claimed in claim 6, wherein the adjusting means comprise: a clock generator for generating clock pulses; an up/down counter for generating control signals to adjust the step AGC amplifier ; means for passing said clock pulses to said up/down counter only during said vertical synchronization interval.

8. (New) An integrated tuner as claimed in claim 7, wherein the adjusting means further comprise: a level detector coupled to an output of the step AGC amplifier; and a

dual comparator coupled to an output of said level detector to provide up/down control signals to said up/down counter in dependence on an output signal of said level detector.

9. (New) An integrated tuner as claimed in claim 8, wherein the level detector continuously measures a total power of all signals in all channels applied to the step AGC amplifier.

10. (New) A receiver comprising: an integrated tuner as claimed in claim 6; and an IF demodulation circuit for providing a vertical sync signal to the integrated tuner.